APPLICATION NOTE

ABSTRACT
Brief set-up routine for using the automatic ‘turn-around’ feature for transceiver control when using the RS-485 (sometimes called 9-bit or multi-drop mode) protocol.

An interrupt may be generated at the time of turn-around.

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This note applies to the following Philips UARTs:
SCN2681, SCN2681T, SCN68681, SCC2691, SCC2692, SCC68692, SCC2698B, SC26C92, SC28L91, SC28L92, SC28C94, SC28L194, SC28L198, SC28L202.

AN10251
Automatic ‘485’ turn-around

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Background

All Philips Industrial UARTs have multi-purpose input and output ports that that may be configured drive static logic levels (control panel indicators for example) or dynamic signals (RTS/CTS flow control, DMA interface signaling, Modem control, internal clocks or interrupts). In general, the output ports drive static levels that are the logical inverse of a register called the OPR (Output Port Register). Under program control these ports may be conditioned to provide other signals such as those mentioned above and the RS–485 control—the subject of this note.

Purpose of the Auto 485 feature

When in a simplex mode of communication is used it becomes necessary for a transceiver device to change its ‘direction’ of communication from transmitting to receiving. This is similar to the function of the ‘push to talk’ switch on a hand held radio. The industrial UARTs provide an automatic control means for this function, based on the end of the message, so that software is not required to monitor when the transmission of a message ends.

The purpose here is to configure the output pins such that they may be controlled by the transmitter of the desired channel. The output pins have slightly different names. They are OP (Output), I/O (Input/Output), IP (Input), MPO (Multi-Purpose Output) and MPI (Multi–Purpose Input). The control is particular to each channel on multi channel devices so that any or all may use this feature as desired.

Programming

It is the Tx control of the output pin that we want.

The programming suggested below is in addition to the normal initialization and control and may be enabled or disabled at any time. It is possible for a system to need the 485 control in some cases and another ‘standard’ in others. It is not inconceivable that some applications may use RTS/CTS flow control as wells as the 485 mode.

The polarity of the OP pins for the Auto 485 feature is logical LOW (V_{SS}) when transmitting, and logical HIGH (V_{CC}) when receiving. Some transceiver devices use the opposite polarity.

The data sheet refers to output pin as the RTSn signal. This, unfortunately, causes some confusion since the pins may be controlled by the command register, the OPR register or the individual receivers or transmitters. When controlled by the receivers the OP pin represents the RTSn flow control. When controlled by the transmitters it signals the end of transmission of the present data block and may also switch the transceiver.

Please note the programming of MR2 bit 5. This bit allows the transmitter to control the OP or I/O pin(s) used for the RTS function. Proper programming will allow the transmitter to drive this pin HIGH about 1 bit time after the completion of the last stop bit of the last character loaded to the TxFIFO. This method allows for the normal ‘under-run’ of the transmitter by the requirement that the Tx be disabled (**not** reset) after the last character of the message is loaded to the Tx FIFO. The make up of a message to be transmitted may not be a continuous data stream—as from a keyboard or a long interrupt latency.

Start:

```
 1. MR1[7]     to  0    Disable Rx control of OP
 2. MR2[5]     to  1    Enable Tx control of OP
[3. IOPCR(1:0) to 01    Set OP pin to output 4 and 8 channel only]
 4. CR         to 0x84  Use command register to set OP low, enable Tx.
 5. Load Tx FIFO        Data need not be continuous, as in keyboard data
 6. CR         to 0x08  After loading the last data byte x disable.
```

End. (For interrupt generation see below)

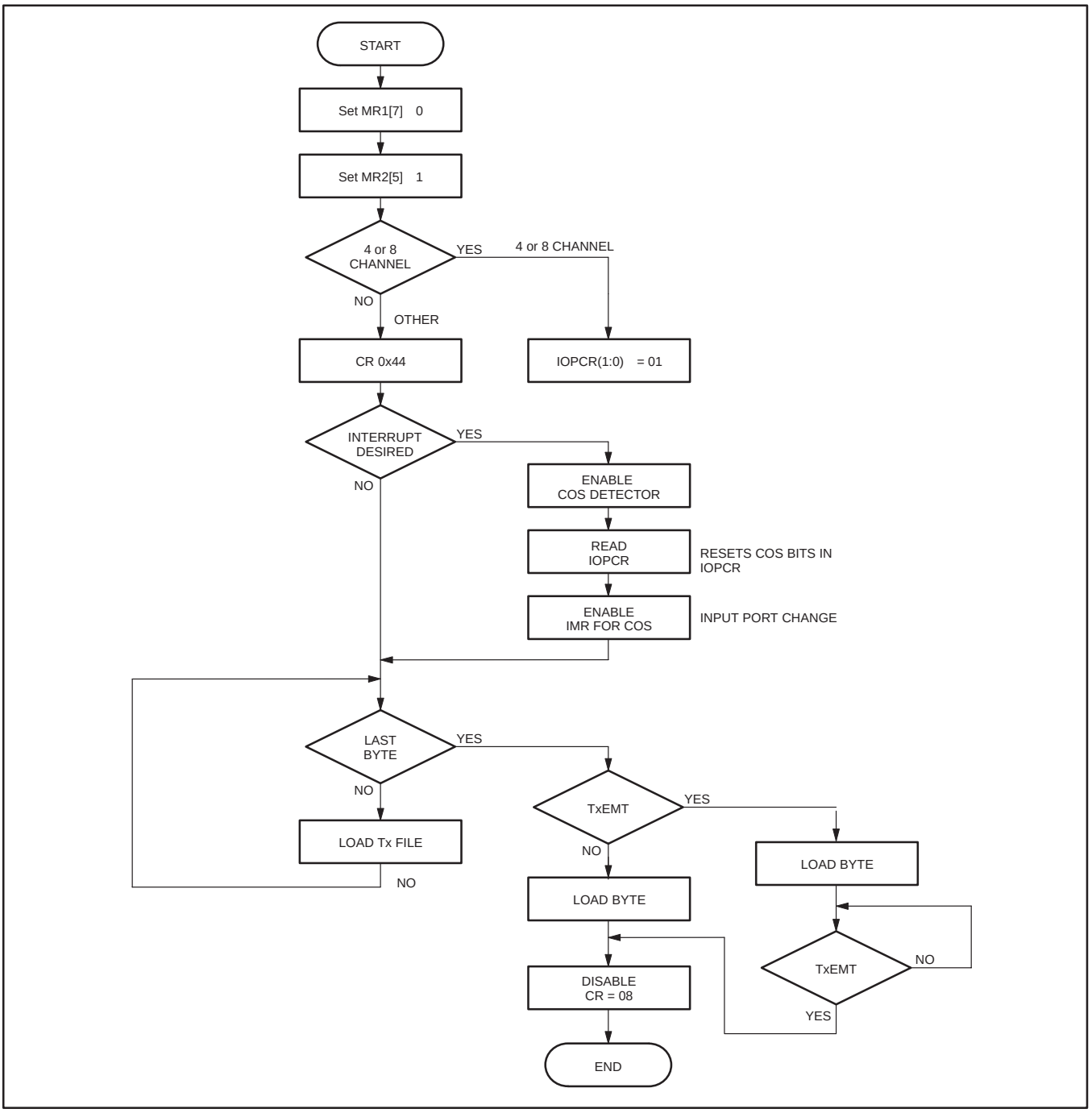

Figure 1. Flow chart

The Tx will now send all the remaining bytes in the Tx FIFO and when it has finished transmitting the last stop bit of the last byte of the last character it will drive the OP pin HIGH. At this time any Tx interrupts will be disabled and Tx status register bits will be cleared. Thus **no** interrupt will be generated at the message end.

The software control will usually expect some response from the system to which it was transmitting, but is not in any way required. That is a system consideration and above the level of this note and hardware.

To send another block all that is required is to drive the OP pin LOW with another 0x80 sent to the CR (Command Register) to drive the OP pin LOW; a return to step 4 above.

Interrupt generation

If an interrupt is desired it may be obtained at the time of turn-around. The method involves enabling a change of state (COS) detector at the output pin. For one and two channel devices this requires the connection of the OP (output) pin to and IP (input) pin and then enabling the change of state detector for the input pin and its interrupt in the IMR (Interrupt Mask Register).

The four and eight channel devices have I/O pins (input/output). On these pins the input is always active even when defined as an output. Therefore the interrupt may be generated my merely enabling the change of state detector and its interrupt for the I/O pin being used.

Thus you are able to get the interrupt and/or the automatic turn-around.

Short message consideration (short version)

When the message is short, sending only one byte for example, delay issuing the disable command to the command register (CR to 0x08) until the TxRdy (or the Tx interrupt) becomes active.

Note: The ‘short message’ consideration may also occur at the end of a transmission block when only one of two more bytes remain to be sent.

Detailed consideration

This involves the disabling of the Tx. The design of the ‘automatic turn-around’ control quite strongly implies that the Tx under-run will not occur—of course an oversight. It is possible that the Tx is under-run when the last byte is loaded to the Tx FIFO or the message is only one byte long. Disabling of the Tx immediately after the loading of that one byte may result in that byte not being sent.

If the Tx is under-run you will see the TxRdy **and** TxEMT bits set in the status register. Loading a byte to the Tx will cause the TxRdy and TxMT to extinguish. Do not issue the Tx disable until the TxRdy goes active again. This will be up to one bit time.

The reason for the above

When the Tx under-runs the Tx state machine returns to state ‘0’ the ‘enabled and idle’ state. The 1×, 16× and X1 clocks control the state machine. The state machine will require one or more of these to move from state ‘0’ to state ‘1’. State ‘1’ is the transmission of the start bit. It is during this time that the data is transferred from the TxFIFO to the shift register. So at the end of the start bit the Tx FIFO will become empty again and the Tx is then ‘busy’. The disable must be issued during the ‘busy’ time of the Tx. The busy time exists when the Tx is enabled and the TxEMT bit is not set.

In other words, issuing the disable when the TxEMT bit is OFF will be safe.

For further information please contact:

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REVISION HISTORY

Rev	Date	Description
_2	20031027	**Application note (9397 750 12206). Supersedes data of 2003 Oct 17 (9397 750 12045).** Modifications: • page 1 and page 4: correct email address for support to: **Datacom.tech-support@philips.com**
_1	20031017	**Application note, initial version (9397 750 12045).**

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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